AMENDMENTS TO THE SPECIFICATION

Please add the following **new** paragraph after the paragraph ending on page 6 line 8:

In the following FIGS. 1-16 the one-hundred series reference numbers, i.e. reference numbers between 100-199, refer to elements introduced in FIG. 1 and the accompanying portion of the Specification, the two-hundred series reference numbers refer to elements introduced in FIG. 2, and so forth up to and including the sixteen-hundred series reference numbers which refer to elements introduced in FIG. 16.

Please replace the paragraph beginning at page 7, line 1 with the following amended paragraph:

FIG. 2 depicts a more detailed view of a representative one of the central offices shown in FIG. 1 including both digital subscriber line access modules (DSLAMs) and PSTN voice band modules. The CO 100 includes subscriber line connections to subscribers 110-114. Each of these connections terminates in the frame room ~~200~~ 201 of the CO. From this room connections are made for each subscriber line via splitters and hybrids to both a DSLAM 202 and to the voice band racks 204. The splitter shunts voice band communications to dedicated line cards, e.g. line card 242 or to a voice band modem pool (not shown). The splitter shunts higher frequency xDSL communications on the subscriber line to a selected line card 210 within DSLAM 202. The line cards of the current invention are universal, meaning they can handle any current or evolving standard of xDSL and may be upgraded on the fly to handle new standards.

Please replace the paragraph beginning at page 7, line 14 with the following amended paragraph:

Voice band call set up is controlled by a Telco switch matrix 240 such as SS7~~.~~ coupled to the PSTN 260. This switch matrix makes point-to-point connections to other subscribers for voice band communications. The xDSL communications may be processed by a universal line

card such as line card 212. That line card includes a plurality of AFE's 212 each capable of supporting a plurality of subscriber lines. The AFEs are coupled via a proprietary packet based bus 214 to a DSP 216 which is also capable of multi-protocol support for all subscriber lines to which the AFE's are coupled. The line card itself is coupled to a back-plane bus 218 which may in an embodiment of the invention be capable of offloading and transporting low latency xDSL traffic between other DSPs for load balancing. Communications between AFE's and DSP(s) are packet based which allows a distributed architecture such as will be set forth in the following FIG. 3 to be implemented. Each of the DSLAM line cards operates under the control of a DSLAM controller 200 which handles global provisioning, e.g. allocation of subscriber lines to AFE and DSP resources. Once a xDSL connection is established between the subscriber and a selected one of the DSLAM submodules, e.g. AFE and DSP the subscriber will be able to access any network to which the DSLAM is connected. In the example shown the DSLAM couples via server 230 with Internet 140.

Please replace the paragraph beginning at page 8, line 9 with the following amended paragraph:

The details of that bus will be set forth in greater detail in the following FIGS. 4-7. AFE Line cards 320,324 each include a plurality of AFEs, e.g. AFEs 322 and 326, respectively each AFE line card is coupled to at least one subscriber line. Each of the line cards also couples to DSP bus 310A. DSP line card 328 includes at least one DSP, e.g. DSP 330. The DSP also couples to DSP bus 310A. Upstream raw digital data from subscribers 110 or 112 is digitized by a corresponding one of AFE's 322 or 326 and passed in packet form onto DSP bus 310A for processing by a requesting one of the DSP's on line card 328. When multiple DSP's are accessing the bus they may have their access arbitrated by a bus arbitrator 340 present on line card 332. This line card couples to both the DSP bus 310A as well as the ATM bus. Line card 346, is a universal line card which contains multiple AFE's e.g. AFE 348 coupled via an on card DSP bus 350 to a DSP 352 on the line card. The AFEs are coupled via xDSL subscriber lines to subscriber 114. ATM data provided from bus 312A to this line card passes directly to a corresponding one of subscribers, e.g. subscriber 114. Raw data on DSP bus 310A may be routed beyond CO 100, e.g. to CO 102 for processing by a corresponding line card with DSP resources in that office as well. Such load balancing would be equally appropriate assuming a

gigabit fiber link between CO/DLC/ONU. Such routing is accomplished by a bridge module 344 on line card 342. The bridge module wraps raw data packet 302 received from an AFE line card, e.g. line card 320, with an appropriate ATM header and sends the wrapped packet 304 across an ATM access card 360 to a corresponding access card (not shown) in CO 102. In that office data is transferred across ATM bus 312B via bridge 364 on line card 362 to DSP bus 310B. From that bus the DSP line card 366 and specifically a requesting DSP 368 processes the raw data and reroutes it back to the ATM network. In still another embodiment of the invention device packets 300 are utilized to control channel flow and control parameters within the various submodules of a DSP. This latter embodiment enables multipath, multiprotocol xDSL support within each DSP. This packet structure and the processes for handling it will be set forth in detail in the following FIGS. 4, 13 and 15.

Please replace the paragraph beginning at page 10, line 7 with the following amended paragraph:

Control of the ~~transmit~~ receive modules, e.g. DMT engine 400 and De-Framer Decoder 402 as well as submodules thereof is implemented as follows. The core processor 424 has DMA access to the FIFO buffer 414 from which it gathers statistical information on each channel including gain tables, or gain table change requests from the subscriber as well as instructions in the embedded operations portion of the channel. Those tables 422 are stored by the core processor in memory 420. When a change in gain table for a particular channel is called for the core processor sends instructions regarding the change in the header of the device packet for that channel via PAD 418 and writes the new gain table to a memory which can be accessed by the appropriate module, i.e. DMT module 400 or the appropriate submodule thereof as a packet corresponding to that channel is received by the module. This technique of in band signaling with packet headers allows independent scheduling of actions on a channel by channel basis in a manner which does not require the direct control of the core processor. Instead each module in the transmit path can execute independently of the other at the appropriate time whatever actions are required of it as dictated by the information in the device header which it reads and executes.

Please replace the paragraph beginning at page 11, line 24 with the following amended paragraph:

A packet on the bus 310A directed to AFE 324 is detected by AFE MAC 474 on the basis of information contained in the packet header. The packet is passed to PAD 476 which removes the header 448 and sends it to the core processor 482 and the packet header information including channel ID to the core processors memory 478. The information is contained in a table 480. The raw data 450 is passed to a FIFO buffer 468 under the control of controller 464. Each channel has a memory mapped location in that buffer. The interpolator 452 reads a fixed amount of data from each channel location in the FIFO buffer. The amount of data read varies for each channel depending on the bandwidth of the channel. The amount of data read during each bus interval (See FIG. 5) is governed by entries in the control table 480 for each channel which is established during channel setup using information contained in a bus packet 302 which contains control parameters for the channel. The interpolator upsamples the data and low pass filters it to reduce the noise introduced by the DSP. Implementing interpolation in the AFE as opposed to the DSP has the advantage of lowering the bandwidth requirements of the DSP bus 310A. From the interpolator data is passed to the FIFO buffer 470 under the control of controller 466. The packets 472 have increased in size as a result of the interpolation. The next module in the transmit pipeline is a DAC 454 which processes each channel in accordance with commands received from the core processor 482 using control parameters downloaded to the control table 480 during channel setup. The analog output of the DAC is passed via analog mux to a corresponding one of sample and hold devices 458. Each sample and hold is associated with a corresponding subscriber line. The sampled data is filtered in analog filters 460 and amplified by line amplifiers 462. The parameters for each of these devices, i.e. filter coefficients, amplifier gain etc. are controlled by the core processor using the above discussed control table 480 and the appropriate parameters stored therein during session set up. For example, where successive packets carry packets with G.Lite, ADSL, and VDSL protocols the sample rate of the analog mux 456 the filter pareameters for filter 460 and the gain of the analog amplifiers will vary for each packet. This "on the fly" configurability allows a single transmit or receive pipeline to be used for multiple concurrent protocols.

Please replace the paragraph beginning at page 13, line 18 with the following amended paragraph:

FIGS. 6A-B are detailed structural views of the receive and transmit packets 302 respectively for transport of data on the system bus shown in FIG. 5. The transmit packet comprises a header 600 and a payload portion 602. The header includes fixed length fields 604-614. Field 604 records the channel or control register address. Field 614 is the read/write field. If the field is set with a read bit the DSP is requesting data from the AFE. The data 616 may be channel data or information from a specific module within the AFE. These latter requests are register requests. A register is the memory location where control parameters for a module are stored. They are memory mapped and are part of control table 480 (See FIG. 4). Alternately, if field 614 is set with a write bit the ~~received~~ transmit packet's ~~data~~ payload portion 602 contains data to be written to a corresponding channel or register. If the data is written to a channel it is communicated through the AFE transmit path for that channel to the subscriber. If the data is written to a register it is communicated to one or more of the modules in the transmit/receive path for processing a particular channel. The DSP ID field 606 is an optional identification field useful when more than one DSP can access the DSP bus. The AFE ID field 608 is used to target a specific AFE on the bus for processing of the packet. When the AFE MAC 474 (See FIG. 4) detects this field it accepts the packet from the bus. The transmit length field 610 indicates for write operations how much data the AFE will expect in the payload portion 602 of the packet. The receive length accompanies a read request in field 614 and indicates how much data the AFE should pass to the requesting DSP.

Please replace the paragraph beginning at page 14, line 5 with the following amended paragraph:

The receive packet passes from the AFE to the corresponding DSP on bus 310A. The bus is bi-directional. The receive packet contains a header 620 and a payload 622. The header contains fields 626,628 and 630 for indicating the receiving DSP, the sending AFE, and the length of the payload in the packet, respectively. Optionally the packet may contain a

channel/register address field 624 for correlating the payload with a specific channel and register. Where a single DSP masters the bus 310A this field may not be required.

Please replace the paragraph beginning at page 16, line 1 with the following amended paragraph:

In FIG. 8A processing for the DSP I/O interface begins at start block 800 in which the DSP I/O interface including PAD 418 FIFO buffer controllers 404,438 and DSP MAC 416 (See FIG. 4) are enabled. Control is passed to decision block 806 in which a determination is made as to the status of bus valid signal line 702 (See FIG. 7A). When that determination is in the affirmative control is passed to process block 808 in which the bus valid signal line is asserted, after which control is passed to decision block 812. In decision block 812 a determination is made based on the channel schedule received from the core processor 424 and/or stored in schedule table 422 as to whether the next scheduled bus transaction for the DSP is a Tx or Rx. If the scheduled operation is a transmit then the PAD 418 gets the next packet to be transmitted from FIFO controller 438 and appends the appropriate header with channel ID etc. in process 814. Subsequently control is passed to process 824 in which the bus is released by MAC 416. Alternately, if in decision process 812 an receive operation for a selected channel is indicated control is passed to request block 810 in which the PAD 418 prepares a read request header and places it on the bus. Subsequently control passes to process 816 in which the bus valid signal line is de-asserted. Control is then passed to process 818 in which a wait state is introduced, subsequent to which a determination is made in decision block 820 as to whether the bus has been reasserted by the responding AFE. This may also involve a determination as to whether the received packet has an DSP ID field 626 (See FIG. 6A) which corresponds with that of the receiving DSP. If the determination is affirmative, control passes to process block 822 for receipt of the data which is written to FIFO buffer 410 via controller 404. Control then returns to next block 804 in which the core processor supplies the next channel, address, state (Tx/Rx) and other information to the PAD in process 802. Control then returns to decision block 806.

Please replace the paragraph beginning at page 16, line 24 with the following amended paragraph:

In FIG. 8B processing for the AFE I/O interface is set forth. That interface includes AFE MAC 474, PAD 476 and FIFO controllers 464,496 and associated buffers 468,502. Processing begins at start block 850 from which control passes to decision process 852. In decision process 852 a determination is made by the AFE MAC as to whether the Bus Valid signal line is asserted. In the event of an affirmative determination control is passed to process 854. In process 854 the header is read and in the following decision process 856 a determination is made as to whether the AFE ID 606 (See FIG. 6B) in the header matches the AFE ID. In the event of an affirmative decision control is passed to decision block 858. In decision block 858 a determination is made as to whether a read or write tag is present in header field 614 (See FIG. 6B). If a read operation is indicated then control passes then the AFE MAC asserts 860 the bus valid signal line after which control passes to decision block 862. In decision block 862 the address field 604 in the header (See FIG. 6B) is read to determine whether a register or channel access is requested by the DSP. If a read register request has been indicated then in processes 864-870 the address to be read, the length of the data to be read and the actual reading and packetizing of the data on the bus with the appropriate header are implemented by the combined AFE I/O interface components. Subsequently, control passes to process 888 in which the bus is deasserted and control is passed to next block 896.

Please replace the paragraph beginning at page 18, line 4 with the following amended paragraph:

FIGS. 11A-C show data structures associated with the management and provisioning of xDSL communications according to an embodiment of the current invention. In FIG. 11A the global allocation table 1100 and the global resource table 1102 are shown. These indicate representative information available to the DSLAM controller 200 (See FIG. 2) for controlling the DSLAM line cards associated with the current invention. The global resource table contains information contains device specific information on operating capabilities and configurability of each resource in the DSLAM and may contain similar information for a

global cluster of DSLAMs at more than one CO or remote access terminal. With this table the controller can intelligently target new channels to existing resources based on parameters. One of those parameters is the line codes supported by the device. Another is the ability of the device to upgrade itself with new parameters corresponding to new xDSL standards.

Please replace the paragraph beginning at page 19, line 1 with the following amended paragraph:

FIG. 11C shows the local allocation and configuration parameter tables 1120 –1122 respectively, associated with the AFE core processor control table ~~422~~ 480. The allocation table contains physical and logical mapping and the protocol, e.g. ADSL, G.Lite, VDSL, associated with each physical/logical channel. The configuration parameter table contains parameters such as sample rate, filter coefficients etc. to be implemented by specific modules within the transmit or receive path for each module in the AFE.

Please replace the paragraph beginning at page 19, line 7 with the following amended paragraph:

FIG. 12 is a candlestick diagram showing communications between a subscriber and a network during initial, setup, and run phases according to an embodiment of the current invention. During the initial phase of provisioning a selected DSP to support a new channel all or part of the Local allocation table 1100 and the configuration parameter table 1112 may be downloaded 1200-1202 from the DSLAM controller 200 to the targeted DSP and stored in core processor memory 420. Next, the DSP I/O interface may download all or part of the Local Allocation or Local Configuration parameters to the targeted AFE for the new channel. The AFE I/O interface accepts a packet transfer if the header in the DSP bus packet 302 matches 1204 the ID of the targeted AFE. Then the AFE stores the configuration parameters for the new channel in the control table ~~470~~ 480 (See FIG. 4).

Please replace the paragraph beginning at page 19, line 17 with the following amended paragraph:

Next setup of the channel is accomplished in accordance with whichever parameter the channel implements. This involves a setup handshake 1206-1208 of transmission and response between the DSP and the modem at the subscriber premise after which the subscriber line is characterized and the channel bit allocation and gains are established. If the channel is available that information may be used to update 1210 the Global Allocation table in the controller. When the setup is finished 1212, control passes to the run time operation.

Please replace the paragraph beginning at page 19, line 23 with the following amended paragraph:

Run time involves the round robin or related processing of successive packets for each channel, including a mix of protocols, with appropriate time segments allocated to each by the DSP and AFE. Each transmission 1220-1222 of data from the DSP to Subscriber is accomplished across the DSP bus through the transmission of a packet to the AFE and the detection and acceptance by the AFE of those packets with a header AFE ID corresponding to that of the targeted device. Upstream communications are requested by the associated DSP and transferred in response by the targeted AFE. When an idle is detected 1224 through either an in band or out of band signal by either the AFE or DSP that state will be updated 1226 in the local allocation table in the DSP and additionally updated 1228 in the Global resource table of the DSLAM controller.

Please replace the paragraph beginning at page 20, line 1 with the following amended paragraph:

FIG. 13A-B are detailed structural views of the device packets 300 utilized in the DSP for the transport of data between various submodules of the DSP shown in FIG. 4. The device packets include a header portion 1300, a command portion 1302 and a payload ~~1302~~ 1306. In an embodiment of the invention the header is of a fixed length. The header includes five fields. Field 1320 contains a value corresponding with the size of the packet. Field 1326 identifies the channel associated with the packet. Field 1328 indicates any common operations among modules to be performed on a channel, i.e. active, inactive, idle etc. Field 1322 contains flags for each module in the associated path, i.e. transmit or receive, and a command size field 1324. The command portion 1302 may contain no command blocks or may contain command blocks for one or more of the modules/submodules on the transmit/receive path. In FIG. 13A three command blocks 1330,1332,1334 are shown.

Please replace the paragraph beginning at page 20, line 18 with the following amended paragraph:

As each module receives each packet it performs two operations on the header. An update of the packet data size is performed on every packet when the processes performed by the module, e.g. DFT or IDFT change the size of the payload. The module updates the value in field 1320 with the new packet size. The other operation is only performed when the module receives a module in which its, the modules, unique flag bit in field 1322 is set. If its flag bit is set, the module reads data starting from the start of the command portion 1302 in an amount corresponding with the command size indicated in field 1324. If the command is one to be executed on the current payload then the receiving module makes the changes and processes the payload data ~~1334~~ 1336. If the command sequence is to be performed on a subsequent packet then the module logs the command and frame reference and executes it at the appropriate frame. After reading the command and processing the data, and before transferring the processed device packet to the next module in the queue the detecting module performs the following operations. It deletes its command information effectively by writing the packet out with the succeeding command blocks 1332-1334 moved from the second and third positions to the first and second positions after the header portion 1300 (See FIG. 13B).

Then the module updates both the command size in the command size field 1324 as well as the packet data size 1320.

Please replace the paragraph beginning at page 21, line 3 with the following amended paragraph:

FIG. 14 is a process flow diagram of representative processes associated with an embodiment of the current invention, which processes are executed by various submodules of the DSP shown in FIG. 4 in response to receipt of device packets shown in FIGS. 13 A-B. This command sequence may in alternate embodiments of the invention be implemented on either the DSP or the AFE should timing, scheduling, scalability etc. make it advantageous to do so. Processing begins in start bock 1400 in which control is passed to process 1402 for the receipt of the next packet. Next in process 1404 the common ops field 1328 is read to see if there are any common ops in the header to be executed. Common ops include a state change for a channel, e.g. active-> inactive/idle. Then in process 1406 the command bit in command flag field 1322 is read. If in decision process 1408 a determination is made that the flag bit for the corresponding module is not set then that module executes process 1432. In process 1432 the packet is processed using parameters previously associated with the channel in the modules channel specific lookup table. Next the module updates 1434 the header with the new data size in field 1320 and passes the packet to the next submodule or module or FIFO buffer. Alternately, if in decision process 1408 a determination is made that the flag bit for the module is set control is passed to processes 1410-1414 in which the command is read and the data is read and processed using the new command. Control then passes to processes 1416 and 1418 in which the detected command block is deleted and in which a updates to the header appended to the processed data are made to reflect changes in command size, packet size. Control then returns via next block 1450 to process 1402.

Please replace the paragraph beginning at page 21, line 22 with the following amended paragraph:

FIG. 15 is a process flow diagram of representative processes executed by the DSP shown in FIG. 4. Processing begins at process 1500 subsequent to which downloads 1502 from the DSLAM controller of the Local Allocation and Configuration parameter tables is accomplished. Next in process 1504 the DSP sets an available process time slot for the allocated channel(s) using resident or downloaded parameters associated with the specific protocol, e.g. G.Lite, ADSL, VDSL, required to support the channel. Then Tx & Rx modules are activated in process 1506. Then control is passed to process 1508 to initiate each channel. Control then passes to process 1512 for the download to each AFE of the local allocation and configuration tables relevant to the target AFE. If all channels have been provisioned in a corresponding targeted AFE(s) then decision process 1514 passes control to the setup phase for each channel in process 1516. otherwise control returns through next channel process 1510 for the processing of the next channel. If alternately, provisioning is not complete control returns via process 1518 in which the local allocation and configuration parameter tables for the next channel and its associated target AFE are downloaded.

Please replace the paragraph beginning at page 22, line 19 with the following amended paragraph:

The setup of each channel occurs in process 1620 using configuration parameters appropriate to whichever XDSL protocol each channel will implement as downloaded in processes 1610, 1614, 1616. Until this is complete control is returned by decision process 1622 to next channel process 1618 until all channels have been setup. Control then passes to process 1624 in which transmit and receive operations are conducted in round robin or other repetitive fashion for each channel in processes 1626-1632. Either a new channel or an idle detection among existing channels will be detected in decision processes 1628, 1632 in which event control will be passed to process 1602 for the download of new allocation and configuration parameters from the DSLAM controller.